HP2100 Simulator Usage
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This memorandum documents the HP 2100 simulator.

1   Simulator Files

sim/	scp.h
	sim_console.h
	sim_defs.h
	sim_fio.h
	sim_rev.h
	sim_sock.h
	sim_tape.h
	sim_timer.h
	sim_tmxr.h
	scp.c
	sim_console.c
	sim_fio.c
	sim_sock.c
	sim_tape.c
	sim_timer.c
	sim_tmxr.c
sim/hp2100/	hp2100_cpu.h
	hp2100_cpu1.h
	hp2100_defs.h
	hp2100_fp.h
	hp2100_fp1.h
	hp2100_cpu.c
	hp2100_cpu0.c
	hp2100_cpu1.c
	hp2100_cpu2.c
	hp2100_cpu3.c
	hp2100_cpu4.c
	hp2100_fp.c
	hp2100_fp1.c
	hp2100_dp.c
	hp2100_dq.c
	hp2100_dr.c
	hp2100_ds.c
	hp2100_ipl.c
	hp2100_lps.c
	hp2100_lpt.c
	hp2100_mt.c
	hp2100_ms.c
	hp2100_mux.c
	hp2100_stddev.c
	hp2100_sys.c

2   HP2100 Features

The HP2100 simulator is configured as follows:

```
        device names        simulates
```

```
        CPU              2114C CPU with up to 16KW of memory
                         2115A CPU with up to 8KW of memory
                         2116C CPU with up to 32KW of memory
                         2100A CPU with up to 32KW of memory
                         1000 (21MX) M/E/F-Series CPU with up to 1024KW of memory
                         EAU, FP, IOP, DMS, FFP, and/or DBI microcode extensions
        MP               12581A/12892B memory protect
        DMA0, DMA1       12607B/12578A/12895A direct memory access controller
        DCPC0, DCPC1     12897B dual-channel port controller
        PTR              12597A duplex register interface with 2748 paper tape
                         reader
        PTP              12597A duplex register interface with 2895 paper tape
                         punch
        TTY              12531C buffered teleprinter interface with 2752
                         teleprinter
        LPS              12653A printer controller with 2767 line printer
                         12566B microcircuit interface with loopback connector
        LPT              12845B printer controller with 2607 line printer
        CLK              12539C time base generator
        MUX,MUXL,MUXM    12920A 16-channel terminal multiplexer
        DP               12557A disk controller with four 2871 drives
                         13210A disk controller with four 7900 drives
        DQ               12565A disk controller with two 2883 drives
        DR               12606B fixed head disk controller with 2770/2771 disk
                         12610B drum controller with 2773/2774/2775 drum
        DS               13037D disk controller with eight 7905/7906/7920/7925
                         drives
        MT               12559C magnetic tape controller with one 3030 drive
        MS               13181A magnetic tape controller with four 7970B drives
                         13183A magnetic tape controller with four 7970E drives
        IPLI             12875A interprocessor link, input side
        IPLO             12875A interprocessor link, output side
```

The HP2100 simulator implements several unique stop conditions:

- Decode of an undefined instruction, and STOP_INST is set
- Reference to an undefined I/O device, and STOP_DEV is set
- More than INDMAX indirect references are detected during memory reference address decoding

The LOAD command supports standard absolute binary format. The DUMP command is not implemented.

2.1 CPU

CPU options include choice of model, memory size, and instruction sets. Several microcode options are simulated:

```
        EAU              Extended Arithmetic Unit
        FP               Single-Precision Floating Point
        IOP              2000/Access I/O Processor
        DMS              Dynamic Mapping System
        FFP              Fast FORTRAN Processor
        DBI              Double Integer Instructions
```

The following standard microcode is automatically enabled when the applicable 1000-Series CPU is selected:

```
      EIG               Extended Instruction Group
      FPP               Floating Point Processor
      SIS               Scientific Instruction Set
```

The general command form is:

```
      SET {-F} CPU <option>
```

Options that may be specified are:

```
      SET CPU 2114              2114C CPU
      SET CPU 2115              2115A CPU
      SET CPU 2116              2116C CPU
      SET CPU 2100              2100A CPU
      SET CPU 1000-M            1000 M-Series CPU
      SET CPU 1000-E            1000 E-Series CPU
      SET CPU 1000-F            1000 F-Series CPU
      SET CPU 21MX-M            21MX M-series CPU (same as 1000-M)
      SET CPU 21MX-M            21MX E-series CPU (same as 1000-E)
      SET CPU LOADERENABLE      enable device loader
      SET CPU LOADERDISABLE     disable device loader
      SET CPU EAU               EAU instructions
      SET CPU NOEAU             no EAU instructions
      SET CPU FP                FP instructions
      SET CPU NOFP              no FP instructions
      SET CPU IOP               IOP instructions
      SET CPU NOIOP             no IOP instructions
      SET CPU FFP               FFP instructions
      SET CPU NOFFP             no FFP instructions
      SET CPU DMS               DMS instructions
      SET CPU NODMS             no DMS instructions
      SET CPU DBI               Double Integer instructions
      SET CPU NODBI             no Double Integer instructions
      SET CPU 4K                set memory size = 4K
      SET CPU 8K                set memory size = 8K
      SET CPU 12K               set memory size = 12K
      SET CPU 16K               set memory size = 16K
      SET CPU 24K               set memory size = 24K
      SET CPU 32K               set memory size = 32K
      SET CPU 64K               set memory size = 64K
      SET CPU 128K              set memory size = 128K
      SET CPU 256K              set memory size = 256K
      SET CPU 512K              set memory size = 512K
      SET CPU 1024K             set memory size = 1024K
```

The CPU models and feature applicability are shown in the following table:

Feature	2114C	2115A	2116C	2100A	1000M	1000E	1000F
Max mem	16K	8K	32K	32K	1024K	1024K	1024K
MP	no	no	opt	std	opt	opt	opt
DMA	opt	opt	opt	opt	opt	opt	opt
EAU	no	opt	opt	std	std	std	std
FP	no	no	no	opt	std	std	std
IOP	no	no	no	opt	opt	opt	opt

```
FFP           no      no      no      opt     opt     opt     std
EIG           no      no      no      no      std     std     std
DMS           no      no      no      no      opt     opt     opt
DBI           no      no      no      no      no*     opt     std
FFP/SIS       no      no      no      no      no      no      std
```

      * DBI was not available for the 1000-M, but the simulator supports it for RTE-6/VM.

If a feature is standard for a given CPU, it cannot be disabled; if a feature is not included, it cannot be enabled.

On the 2100, the FP or FFP and IOP options are mutually exclusive. To support CPU detection in the HP diagnostic configurator, the 1000-E/F TIMER instruction decodes as MPY on the 1000-M, and the RRR 16 instruction decodes as NOP on the 2114. The 1000-F FPP supports several undocumented instructions used by the FPP-SIS-FFP diagnostic. All other disabled or unimplemented instructions cause a simulator halt if STOP_INST is set.

Setting the CPU model establishes a consistent set of standard features and common options. Additional SET CPU commands may follow to fine-tune the desired feature set.

The 2114, 2115, 2116, and 2100 models support a protected area of memory containing an initial binary loader. The loader always resides in the highest 64 memory locations, regardless of capacity. Enabling the loader makes this area available. Disabling the loader renders this area non-existent, so that reads from the area return zero, and writes to the area are ignored. The paper tape loader, configured for select code 10, initially resides in this area when the simulator is started.

The initial memory size is set to a maximum of 32K. If the memory size is being reduced, either by setting a smaller size or by changing to a CPU with a smaller memory capacity, and the memory being truncated contains non-zero data, the simulator asks for confirmation before proceeding. The confirmation request may be suppressed by using the "-f" switch. Data in the truncated portion of memory is lost.

These switches are recognized when examining or depositing in CPU memory:

```
    -v                  if DMS enabled, interpret address as virtual
    -s                  if DMS enabled, force system map
    -u                  if DMS enabled, force user map
    -p                  if DMS enabled, force port A map
    -q                  if DMS enabled, force port B map
```

The CPU implements four different kinds of instruction breakpoints:

```
    -e                  break unconditionally
    -n                  break if DMS is disabled
    -s                  break if DMS enabled and system map
    -u                  break if DMS enabled and user map
```

CPU registers include the visible state of the processor as well as the control registers for the interrupt system.

```
    name                models      size    comments

    P                   all         15      program counter
    A                   all         16      A register
    B                   all         16      B register
    M                   all         15      M (memory address) register
    T                   all         16      T (memory data) register
```

```
            X                     1000        16    X index register
            Y                     1000        16    Y index register
            S                     all         16    switch/display register
            E                     all         1     extend flag
            O                     all         1     overflow flag
            ION                   all         1     interrupt enable flag
            ION_DEFER             all         1     interrupt defer flag
            CIR                   all         6     central interrupt register
            DMSENB                1000        1     DMS enable
            DMSCUR                1000        1     DMS current map (1 = user map)
            DMSSR                 1000        16    DMS status register
            DMSVR                 1000        16    DMS violation register
            DMSMAP[128]           1000        16    DMS maps
                                                    [0:31] system map
                                                    [32:63] user map
                                                    [64:95] port A map
                                                    [96:127] port B map
            STOP_INST             all         1     stop on undefined instruction
            STOP_DEV              all         1     stop on undefined device
            INDMAX                all         16    indirect address limit
            PCQ[0:63]             all         15    P of last JMP, JSB, or interrupt;
                                                    most recent P change first
```

BOOT CPU implements the 1000 IBL facility. IBL is controlled by the switch register S. S<15:14> selects the device to boot:

```
            00                    2748B paper-tape reader (12992K ROM)
            01                    7900A/2883 disk (12992A ROM)
            10                    7970B/E tape (12992D ROM)
            11                    13037D disk (12992B ROM)
```

For the 7900A/2883 only, S<13:12> specify the type of disk:

```
            00                    7900A
            10                    2883
```

S<11:6> contains the device address. If the device has two addresses, S<11:6> specifies the lower address. S<5:3> are passed to the bootstrap program. S<2:0> specify options for the boot loader. IBL will not report an error if the device address in S<11:6> is incorrect.

2.2 12581A/12892B Memory Protect

Memory protect is standard equipment on the 2100 (although it may be disabled by removing a jumper) and optional on the 2116 and 1000. The following registers are implemented:

```
            name                  size        comments

            CTL                   1           memory protection enable
            FLG                   1           protection violation flag
            FBF                   1           protection violation flag buffer
            FR                    15          fence register
            VR                    16          violation register
            EVR                   1           enable violation register flag
            MEV                   1           memory expansion (DMS) violation flag
```

The 1000 memory protect card (12892B) has three feature options that are implemented by jumper settings. These are controlled by the following commands:

```
SET MP JSBIN                      jumper W5 installed
SET MP JSBOUT                     jumper W5 removed
SET MP INTIN                      jumper W6 installed
SET MP INTOUT                     jumper W6 removed
SET MP SEL1IN                     jumper W7 installed
SET MP SEL1OUT                    jumper W7 removed
```

W5 determines whether JSB instructions referencing memory locations 0 and 1 are legal (installed) or illegal (removed). W6 controls whether the first three levels of indirect addressing hold off (installed) or permit (removed) pending interrupts. W7 determines whether I/O instructions referencing select codes other than 1 are legal (installed) or illegal (removed); note that I/O instructions referencing select code 1 are legal, and HLT instructions are illegal, regardless of the setting of W7.

The default configuration is JSB (W5) installed, INT (W6) installed, and SEL1 (W7) removed, providing compatibility with the 2116 and 2100 memory protect cards.

2.3 12607B/12578A/12895A DMA Controllers, 12897B DCPC Controller

The direct memory access/dual channel port controller is an option for all CPUs. The 12607B DMA controller provides one channel, DMA0, on the 2114. The other DMA/DCPC controllers provide two channels (DMA0 and DMA1 on the 2115, 2116, and 2100, or DCPC0 and DCPC1 on the 1000). Each channel has the following visible state:

```
name            size        comments

CMD             1           channel enabled
CTL             1           interrupt enabled
FLG             1           channel ready
FBF             1           channel ready buffer
CTLALT          1           command word 2/3 selector
CW1             16          command word 1
CW2             16          command word 2
CW3             16          command word 3
LATENCY         8           first-cycle delay
BYTE            1           even/odd byte-packing flag
PACKER          8           byte-packing register
```

2.4 Variable Device Assignments

On the HP2100, I/O devices take their device numbers from the backplane slot they are plugged into. Thus, device number assignments vary considerably from system to system, and software package to software package. The HP2100 simulator supports dynamic device number assignment. To show the current device number, use the SHOW <dev> DEVNO command:

```
sim> SHOW PTR DEVNO
device=10
```

To change the device number, use the SET <dev> DEVNO=<num> command:

```
sim> SET PTR DEVNO=30
sim> SHOW PTR DEVNO
device=30
```

The new device number must be in the range 010..077 (octal). For devices with two device numbers, only the lower numbered device number can be changed; the higher is automatically set to the lower + 1. If a device number conflict occurs, the simulator will return an error when program execution is started.

2.4.1 Device State

All devices other than the CPU and TTY may be disabled or enabled. Disabling a device simulates removing the associated interface from the CPU card cage. To disable or enable a device, use:

```
SET <dev> DISABLED              disable device
SET <dev> ENABLED               enable device
```

For devices with more than one device number, disabling or enabling any device in the set disables or enables all of the devices.

Devices consisting of multiple addressable units connected to a controller typically allow the units to be individually enabled or disabled. Disabling simulates disconnecting the associated unit from the controller. The commands to set units enabled and disabled are:

```
SET <unit> DISABLED             disable unit
SET <unit> ENABLED              enable unit
```

Some devices and units allow simulation of power-down conditions. Power settings are controlled by these commands:

```
SET <dev> POWEROFF              turn power off
SET <dev> POWERON               turn power on
```

Peripherals that provide operator-selectable disconnection, typically via an "offline" switch, provide these simulation equivalents:

```
SET <dev> OFFLINE               set peripheral offline
SET <dev> ONLINE                set peripheral online
```

2.5 Programmed I/O Devices

2.5.1 12597A-002 Duplex Register Interface (PTR) with 2748 Paper Tape Reader

The paper tape reader (PTR) reads data from a disk file. The POS register specifies the number of the next data item to be read. Thus, by changing POS, the user can backspace or advance the reader.

For diagnostic purposes, a tape loop may be simulated with the commands:

```
SET PTR DIAG                    rewind tape at EOF
SET PTR READER                  supply tape trailer at EOF
```

The paper tape reader supports the BOOT command. BOOT PTR copies the IBL into memory and starts it running. The switch register (S) is set automatically to the value expected by the IBL loader:

```
<15:12>     =       0000
<11:6>      =       device code
<5:3>       =       unchanged
```

```
        <2:0>        =        000
```

The paper tape reader implements these registers:

```
        name            size          comments

        BUF             8             last data item processed
        CMD             1             reader enable
        CTL             1             device/interrupt enable
        FLG             1             device ready
        FBF             1             device ready buffer
        SRQ             1             device DMA service request
        TRLLIM          8             number of trailing nulls to append
                                      after end-of-file is detected
        POS             32            position in the input file
        TIME            24            time from I/O initiation to interrupt
        STOP_IOE        1             stop on I/O error
```

The TRLLIM register specifies the number of nulls to supply as paper tape trailer when EOF is detected. If TRLLIM is set to zero or the count is exhausted, the reader will hang.

Error handling is as follows:

```
        error           STOP_IOE      processed as

        not attached    1             report error and stop
                        0             out of tape

        end of file     1             report error and stop
                        0             out of tape

        OS I/O error    x             report error and stop
```

2.5.2 12597A-005 Duplex Register Interface (PTP) with 2895 Paper Tape Punch

The paper tape punch (PTP) writes data to a disk file. The POS register specifies the number of the next data item to be written. Thus, by changing POS, the user can backspace or advance the punch.

The paper tape punch implements these registers:

```
        name            size          comments

        BUF             8             last data item processed
        CMD             1             punch enable
        CTL             1             device/interrupt enable
        FLG             1             device ready
        FBF             1             device ready buffer
        SRQ             1             device DMA service request
        POS             32            position in the output file
        TIME            24            time from I/O initiation to interrupt
        STOP_IOE        1             stop on I/O error
```

Error handling is as follows:

```
error           STOP_IOE        processed as

not attached    1               report error and stop
                0               out of tape

OS I/O error    x               report error and stop
```

2.5.3 12531C Buffered Teleprinter Interface (TTY) with 2752 Teleprinter

The console teleprinter has three units: keyboard (unit 0), printer (unit 1), and punch (unit 2). The keyboard reads from the console keyboard; the printer writes to the simulator console window. The punch writes to a disk file. The keyboard and printer units (TTY0, TTY1) can be set to one of four modes: UC, 7P, 7B, or 8B:

```
mode  input characters        output characters

UC    lower case converted    lower case converted to upper case,
      to upper case,          high-order bit cleared,
      high-order bit cleared  non-printing characters suppressed
7P    high-order bit cleared  high-order bit cleared,
                              non-printing characters suppressed
7B    high-order bit cleared  high-order bit cleared
8B    no changes              no changes
```

The default mode is UC.

Some HP software systems expect the console to transmit line-feed automatically following carriage-return. This feature is enabled with:

```
SET TTY AUTOLF
```

and disabled with:

```
SET TTY NOAUTOLF
```

The console teleprinter implements these registers:

```
name            size        comments

BUF             8           last data item processed
MODE            16          mode
CTL             1           device/interrupt enable
FLG             1           device ready
FBF             1           device ready buffer
SRQ             1           device DMA service request
KPOS            32          number of characters input
KTIME           24          keyboard polling interval
TPOS            32          number of characters printed
TTIME           24          time from I/O initiation to interrupt
PPOS            32          position in the punch output file
STOP_IOE        1           punch stop on I/O error
```

Error handling for the punch is as follows:

```
error           STOP_IOE        processed as

not attached    1               report error and stop
```

```
                          0              out of tape

OS I/O error      x              report error and stop
```

2.5.4 12653A Printer Controller (LPS) with 2767 Line Printer, 12566B Microcircuit Interface with Loopback Connector

The 2767 line printer uses the 12653A line printer interface as its controller. As a line printer, LPS writes data to a disk file. The POS register specifies the number of the next data item to be written. Thus, by changing POS, the user can backspace or advance the printer.

The line printer responds to SET LPS POWEROFF as if the power were removed or the printer cable were disconnected, and to DETACH LPS as if the paper were out. It also provides these additional state commands:

```
    SET LPS OFFLINE              simulate ONLINE button up
    SET LPS ONLINE               simulate ONLINE button down
    SET LPS REALTIME             use realistic timing for print operations
    SET LPS FASTTIME             use optimized timing for print operations
```

As a 12566B microcircuit interface, LPS provides the test device for running several of the HP diagnostics. Printer mode versus diagnostic mode is controlled by the commands:

```
    SET LPS PRINTER              configure as line printer
    SET LPS DIAG                 configure for diagnostic tests
```

In diagnostic mode, LPS simulates the installation of the HP 1251-0332 diagnostic test (loopback) connector onto the 12566B card and the setting of the appropriate card jumpers for the diagnostic.

LPS may be configured to send debugging information to the previously enabled debug output device using these commands:

```
    SET LPS DEBUG                provide debug printouts
    SET LPS NODEBUG              inhibit debug printouts
```

Diagnostic information includes characters supplied to and status received from the interface, as well as data transfer initiations and completions.

The 12653A is disabled by default.

The 12653A implements these registers:

```
    name              size          comments

    BUF               16            output buffer
    STA               16            input buffer or status
    POWER             2             printer power state
    CMD               1             printer enable
    CTL               1             device/interrupt enable
    FLG               1             device ready
    FBF               1             device ready buffer
    SRQ               1             device DMA service request
    CCNT              7             current character count
    LCNT              7             current line count
    POS               32            position in the output file
```

```
        CTIME            24              character transfer time
        PTIME            24              per-zone print operation time
        STIME            24              per-line paper slew time
        RTIME            24              power-on ready delay time
        STOP_IOE         1               stop on I/O error
```

In printer mode, error handling is as follows:

```
        error           STOP_IOE        processed as

        not attached    1               report error and stop
                        0               out of paper

        SET POWEROFF    1               report error and stop
                        0               powered off

        SET OFFLINE     1               report error and stop
                        0               offline

        OS I/O error    x               report error and stop
```

With STOP_IOE set to 0, output performed when the device is powered off or offline will initiate but then hang, waiting for the device to be returned online. When it is, the output operation will complete.

In diagnostic mode, there are no errors; data sent to the output buffer is looped back to the status register immediately.

2.5.5 12845B Printer Controller (LPT) with 2607 Line Printer

The line printer (LPT) writes data to a disk file. The POS register specifies the number of the next data item to be written. Thus, by changing POS, the user can backspace or advance the printer.

The line printer responds to SET LPT POWEROFF as if the power were removed or the printer cable were disconnected and DETACH LPT as if the paper were out. It also provides these additional state commands:

```
        SET LPT OFFLINE                 simulate PAPER button up
        SET LPT ONLINE                  simulate PAPER button down
```

The line printer implements these registers:

```
        name            size            comments

        BUF             8               last data item processed
        CMD             1               printer enable
        CTL             1               device/interrupt enable
        FLG             1               device ready
        FBF             1               device ready buffer
        SRQ             1               device DMA service request
        LCNT            7               line count within page
        POS             32              position in the output file
        CTIME           24              time between characters
        PTIME           24              time for a print operation
        STOP_IOE        1               stop on I/O error
```

Error handling is as follows:

```
error          STOP_IOE       processed as

not attached   1              report error and stop
               0              out of paper

SET POWEROFF   1              report error and stop
               0              powered off

SET OFFLINE    1              report error and stop
               0              offline

OS I/O error   x              report error and stop
```

With STOP_IOE set to 0, output performed when the device is powered off or offline will initiate but then hang, waiting for the device to be returned online. When it is, the output operation will complete.

2.5.6 12539C Time Base Generator (CLK)

The time base generator (CLK) may be set for diagnostic mode:

```
SET CLK DIAG                   configure for diagnostic mode
SET CLK CALIBRATED             configure for timing mode
```

Diagnostic mode corresponds to setting jumper W2 to position "B". This turns off autocalibration and divides the longest time intervals down by 1000.

The time base generator implements these registers:

```
name           size           comments

SEL            3              time base select
CTR            14             repeat counter for < 1Hz operation
CTL            1              device/interrupt enable
FLG            1              device ready
FBF            1              device ready buffer
ERR            1              error flag
TIME[0:7]      31             clock intervals, select = 0..7
DEVNO          6              current device number (read only)
```

The time base generator autocalibrates; the clock interval is adjusted up or down so that the clock tracks actual elapsed time. Operation at the fastest rates (100 microseconds, 1 millisecond) is not recommended.

2.5.7 12920A 16-Channel Terminal Multiplexer (MUX, MUXL, MUXM)

The 12920A is a 16-line terminal multiplexer, with five additional receive-only diagnostic lines. It consists of three devices:

```
MUX        scanning logic (corresponds to the upper data card)
MUXL       individual lines (corresponds to the lower data card)
MUXM       modem control and status logic (corresponds to the control
           card)
```

The MUX performs input and output through Telnet sessions connected to a user-specified port. The ATTACH command to the scanning logic specifies the port to be used:

```
        ATTACH MUX <port>              set up listening port
```

where `<port>` is a decimal number between 1 and 65535 that is not being used for other TCP/IP activities.

Each line (each unit of MUXL) can be set to one of four modes: UC, 7P, 7B, or 8B:

```
    mode  input characters       output characters

    UC    lower case converted   lower case converted to upper case,
          to upper case,         high-order bit cleared,
          high-order bit cleared non-printing characters suppressed
    7P    high-order bit cleared high-order bit cleared,
                                 non-printing characters suppressed
    7B    high-order bit cleared high-order bit cleared
    8B    no changes             no changes
```

In addition, each line supports the DATASET option. DATASET, when set, enables modem control. The default settings are UC mode and DATASET disabled. Finally, each line supports output logging. The `SET MUXLn LOG` command enables logging on a line:

```
    SET MUXLn LOG=filename  log output of line n to filename
```

The `SET MUXLn NOLOG` command disables logging and closes the open log file, if any.

The modem controls model a simplified Bell 103A dataset with just four lines: data terminal ready and request to send from the computer to the data set, and carrier detect and data set ready from the data set to the computer. There is no ring detection. If data terminal ready is set when a Telnet connection starts up, then carrier detect and data set ready are also set. The connection is established whether data terminal ready is set or not.

Once MUX is attached and the simulator is running, the multiplexer listens for connections on the specified port. It assumes that the incoming connections are Telnet connections. The connections remain open until disconnected either by the Telnet client, a `SET MUXL DISCONNECT` command, or a `DETACH MUX` command.

Other special multiplexer commands:

```
    SHOW MUX CONNECTIONS          show current connections
    SHOW MUX STATISTICS           show statistics for active connections
    SET MUXLn DISCONNECT          disconnects the specified line.
```

The scanner (MUX) implements these registers:

```
    name            size        comments

    IBUF            16          input buffer, holds line status
    OBUF            16          output buffer, holds channel select
```

The lines (MUXL) implements these registers:

```
    name            size        comments

    CTL             1           device/interrupt enable
    FLG             1           device ready
    FBF             1           device ready buffer
    SRQ             1           device DMA service request
```

```
STA[0:20]          16              line status, lines 0-20
RPAR[0:20]         16              receive parameters, lines 0-20
XPAR[0:15]         16              transmit parameters, lines 0-15
RBUF[0:20]         8               receive buffer, lines 0-20
XBUF[0:15]         8               transmit buffer, lines 0-15
RCHP[0:20]         1               receive character present, lines 0-20
XDON[0:15]         1               transmit done, lines 0-15
TIME[0:15]         24              transmit time, lines 0-15
```

The modem control (MUXM) implements these registers:

```
name               size            comments

CTL                1               device/interrupt enable
FLG                1               device ready
FBF                1               device ready buffer
SRQ                1               device DMA service request
SCAN               1               scan enabled
CHAN               4               current line
DSO[0:15]          6               C2,C1,ES2,ES1,SS2,SS1, lines 0-15
DSI[0:15]          2               S2,S1, lines 0-15
```

The terminal multiplexer does not support save and restore. All open connections are lost when the simulator shuts down or MUX is detached.

2.5.8 12875A Interprocessor Link (IPLI, IPLO)

The interprocessor link is a pair of 12566B parallel interfaces that are cross-coupled to provide interprocessor communications to a second copy of the HP2100 simulator. The IPL is intended to support simulation of a two-system HP TimeShared Basic configuration. The links are actually bidirectional half-duplex; TimeShared Basic uses them unidirectionally. The IPL is disabled by default.

To operate, the IPL devices must be enabled and then connected to the IPL devices in another copy of the simulator. The IPLI device in the first simulator is connected to the IPLO device in the second, and vice versa. Connections are established with the ATTACH command. One copy of the simulator listens for connections on a specified port (ATTACH -L); the other establishes connections to an IP address and port (ATTACH -C). Either copy may perform either operation, but the operations must be done in matched pairs:

```
simulator #1                       simulator #2

sim> set ipli ena                  sim> set ipli ena
(also enables iplo)                (also enables iplo)
sim> att -lw ipli 4000
Listening on port 4000
Waiting for connection
                                   sim> att -c iplo 4000
Connection established             Connected to 127.0.0.1 port 4000
sim> att -lw iplo 4000
Listening on port 4001
Waiting for connection
                                   sim> att -c ipli 4001
Connection established             Connected to 127.0.0.1 port 4000
```

Both forms of ATTACH take a modifier -W (wait); if specified, the command will wait up to 30 seconds for the connection process to complete. ATTACH -C can specify both an IP address and a port, in the form aa.bb.cc.dd:port; if the IP address is omitted, it defaults to 127.0.0.1 (local system).

Both IPLI and IPLO implement the `BOOT` command. `BOOT` loads the HP Access Basic Block Loader for the IOP into the top 64 words of memory and starts it running.

Both IPLI and IPLO implement these registers:

```
name              size            comments

BUF               16              buffer
HOLD              8               holding buffer
CMD               1               device enable
CTL               1               device/interrupt enable
FLG               1               device ready
FBF               1               device ready buffer
SRQ               1               device DMA service request
TIME              24              polling interval for input
STOP_IOE          1               stop on I/O error
```

2.6 Disk Controllers

2.6.1 12557A Disk Controller (DPC, DPD) with Four 2781 Drives, 13210A Disk Controller (DPC, DPD) with Four 7900 Drives

The 12557A/13210A disk controller has two separate devices, a data channel (DPD) and a command channel (DPC). The data channel includes a 128-word (one sector) buffer for reads and writes. The command channel includes the four disk drives. The 12557A/13210A controller can be configured as either a 12557A, supporting 2.5MB drives, or a 13210A, supporting 5MB drives, with the commands:

```
SET DPC 12557A                2.5MB drives
SET DPC 13210A                5.0MB drives
```

Drive types cannot be intermixed; the controller is configured for one type or the other. The 13210A (for 7900/7901 disks) is selected by default.

Individual drives may be protected against writing. These commands simulate the Upper/Lower Disc Protect switches on the drives:

```
SET DPCn LOCKED               set unit n write locked
SET DPCn WRITEENABLED         set unit n write enabled
```

Separate protection for the upper and lower platters of the 7900 drive is not supported. Also, the drive Protect/Override switch is not supported; drive protection is permanently overridden.

Drives may also have their heads unloaded and loaded:

```
SET DPCn UNLOADED             unload heads on unit n
SET DPCn LOADED               load heads on unit n
```

This provides a convenient method of setting a drive "down" without detaching the associated disk image file. Drives can also be set `DISABLED` or `ENABLED`.

The 12557A/13210A supports the `BOOT` command. `BOOT DPC` copies the IBL for 7900 class disks into memory and starts it running. `BOOT -R DPC` boots from the removable platter (head 0). The switch register (S) is set automatically to the value expected by the IBL loader:

```
<15:14>     =       01
<13:12>     =       00
<11:6>      =       data channel device code
<5:3>       =       unchanged
<2:1>       =       00
<0>         =       1 if booting from the removable platter
```

The data channel (DPD) implements these registers:

name	size	comments
IBUF	16	input buffer
OBUF	16	output buffer
DBUF[0:127]	16	sector buffer
BPTR	7	sector buffer pointer
CMD	1	channel enable
CTL	1	interrupt enable
FLG	1	channel ready
FBF	1	channel ready buffer
SRQ	1	channel DMA service request
XFER	1	transfer in progress flag
WVAL	1	write data valid flag

The command channel (DPC) implements these registers:

name	size	comments
OBUF	16	output buffer
BUSY	4	busy (unit #, + 1, of active unit)
CNT	5	check record count
CMD	1	controller enable
CTL	1	interrupt enable
FLG	1	controller ready
FBF	1	controller ready buffer
SRQ	1	controller DMA service request
EOC	1	end of cylinder pending
POLL	1	attention polling enabled
RARC	8	record address register (cylinder)
RARH	2	record address register (head)
RARS	4	record address register (sector)
CYL[0:3]	8	current cylinder, drives 0-3
STA[0:3]	16	drive status, drives 0-3
CTIME	24	data transfer command delay time
DTIME	24	data channel command delay time
STIME	24	seek delay time, per cylinder
XTIME	24	interword transfer time

Error handling is as follows:

error	processed as
not attached	disk not ready (heads unloaded)

```
        end of file         assume rest of disk is zero

        OS I/O error        report error and stop
```

2.6.2 12565A Disk Controller (DQC, DQD) with Two 2883 Drives

The 12565A disk controller has two separate devices, a data channel (DQD) and a command channel (DQC). The data channel includes a 128-word (one sector) buffer for reads and writes. The command channel includes the two disk drives.

Individual drives may be protected against writing:

```
        SET DQCn LOCKED             set unit n write locked
        SET DQCn WRITEENABLED       set unit n write enabled
```

Drives may have their heads unloaded and loaded:

```
        SET DQCn UNLOADED           unload heads on unit n
        SET DQCn LOADED             load heads on unit n
```

This provides a convenient method of setting a drive "down" without detaching the associated disk image file. Disk drives can also be set DISABLED or ENABLED.

The 12565A supports the BOOT command. BOOT DQC copies the IBL for 2883 class disks into memory and starts it running. The switch register (S) is set automatically to the value expected by the IBL loader:

```
        <15:12>     =       0110
        <11:6>      =       data channel device code
        <5:3>       =       unchanged
        <2:0>       =       000
```

The data channel (DQD) implements these registers:

```
        name                size            comments

        IBUF                16              input buffer
        OBUF                16              output buffer
        DBUF[0:127]         16              sector buffer
        BPTR                7               sector buffer pointer
        CMD                 1               channel enable
        CTL                 1               interrupt enable
        FLG                 1               channel ready
        FBF                 1               channel ready buffer
        SRQ                 1               channel DMA service request
        XFER                1               transfer in progress flag
        WVAL                1               write data valid flag
```

The command channel (DQC) implements these registers:

```
        name                size            comments

        OBUF                16              output buffer
        BUSY                2               busy (unit # + 1 of active unit)
        CNT                 9               check record count
        CMD                 1               controller enable
```

```
CTL                    1              interrupt enable
FLG                    1              controller ready
FBF                    1              controller ready buffer
SRQ                    1              controller DMA service request
RARC                   8              record address register (cylinder)
RARH                   5              record address register (head)
RARS                   5              record address register (sector)
CYL[0:1]               8              current cylinder, drives 0-1
HED[0:1]               5              current head, drives 0-1
STA[0:1]               16             drive status, drives 0-1
CTIME                  24             data transfer command delay time
DTIME                  24             data channel command delay time
STIME                  24             seek delay time, per cylinder
XTIME                  24             interword transfer time
```

Error handling is as follows:

```
error               processed as

not attached        disk not ready (heads unloaded)

end of file         assume rest of disk is zero

OS I/O error        report error and stop
```

2.6.3 12606B Fixed Head Disk Controller (DRC, DRD) with 2770/2771 Disk, 12610B Drum Controller (DRC, DRD) with 2773/2774/2775 Drum

The 12606B/12610B fixed head disk/drum controller has two separate devices, a data channel (DRD) and a command channel (DRC). The command channel includes the actual drive. Ten different models are supported:

```
command             interface and size        model

SET DRC 180K        12606B, 180K words        2770A
SET DRC 360K        12606B, 360K words        2771A
SET DRC 720K        12606B, 720K words        2771A-001
SET DRC 384K        12610B, 384K words        2773A
SET DRC 512K        12610B, 512K words        2773A-001
SET DRC 640K        12610B, 640K words        2773A-002
SET DRC 768K        12610B, 768K words        2774A
SET DRC 896K        12610B, 896K words        2774A-001
SET DRC 1024K       12610B, 1024K words       2774A-002
SET DRC 1536K       12610B, 1536K words       2775A
```

The command channel supports write-protected tracks. Track protection is enabled with this command:

```
SET DRC PROTECTED
```

In addition, the number of protected tracks is specified by the command:

```
SET DRC TRACKPROT=count
```

The track protect count must be a power of two from 1 to 128 on the 12606 interface and from 1 to 512, or 768, on the 12610 interface. If the drive has fewer tracks than the track protect count, then all tracks on the drive are eligible for protection.

Track protection is disabled with this command:

```
SET DRC UNPROTECTED
```

The 12606B/12610B support the BOOT command. BOOT DRD loads the first sector from the disk or drum into locations 0-77 and then jumps to 77. This is very different from the IBL loader protocol used by the 12565A and the 12557A/13210A.

The data channel (DRD) implements these registers:

```
name               size           comments


IBUF               16             input buffer
OBUF               16             output buffer
CMD                1              channel enable
CTL                1              interrupt enable
FLG                1              channel ready
FBF                1              channel ready buffer
SRQ                1              channel DMA service request
BPTR               6              sector buffer pointer
```

The command channel implements these registers:

```
name               size           comments


CW                 16             command word
STA                16             status
RUN                1              run flip-flop
CMD                1              controller enable
CTL                1              interrupt enable
FLG                1              controller ready
FBF                1              controller ready buffer
SRQ                1              controller DMA service request
TIME               24             interword transfer time
STOP_IOE           1              stop on I/O error
```

Error handling is as follows:

```
error              processed as

not attached       drum or disk not ready
```

12606B/12610B data files are buffered in memory; therefore, end of file and OS I/O errors cannot occur.

2.6.4 13037D Disk Controller (DS) with Eight 7905/7906/7920/7925 Drives

The 13037D disk controller supports 7905 (15MB), 7906 (20MB), 7920 (50MB), or 7925 (120MB) disk drives, as well as autosizing, based on the size of the disk image file:

```
SET DSn 7905                      drive n is a 15MB drive
SET DSn 7906                      drive n is a 20MB drive
SET DSn 7920                      drive n is a 50MB drive
```

```
        SET DSn 7925                    drive n is a 120MB drive
        SET DSn AUTOSIZE                drive n type based on file size at ATTACH
```

Drive types can be intermixed. The 7905 is selected by default.

Individual drives may be protected against writing. These commands simulate the Disc Protect/Read Only switches on the drives:

```
        SET DSn LOCKED                  set unit n write locked
        SET DSn WRITEENABLED            set unit n write enabled
```

Separate protection for the upper and lower platters of the 7905 and 7906 drives is not supported. Protecting a 7905 or 7906 drive behaves as though both of the Disc Protect switches were on.

Drives may also have their heads unloaded and loaded:

```
        SET DSn UNLOADED                unload heads on unit n
        SET DSn LOADED                  load heads on unit n
```

This provides a convenient method of setting a drive "down" without detaching the associated disk image file.

The setting of the drive Format switch may be changed with:

```
        SET DSn FORMAT                  set format enabled
        SET DSn NOFORMAT                set format disabled
```

Drives can also be set DISABLED or ENABLED.

The 13037D supports the BOOT command. BOOT DS copies the IBL loader for the 13037D controller into memory and starts it running. The switch register (S) is set automatically to the value expected by the IBL loader:

```
        <15:14>      =      11
        <13:12>      =      01
        <11:6>       =      data channel device code
        <5:3>        =      unchanged
        <2>          =      0
        <1:0>        =      unchanged (head number)
```

The DS controller implements these registers:

```
        name                size         comments

        CMD                 16           command register
        FIFO[0:15]          16           data FIFO
        SR1                 16           status register 1
        VCTR                16           verify counter
        FMASK               8            file mask
        CYL                 16           cylinder address register
        HS                  16           head/sector address register
        STATE               2            controller state
        LASTA               3            last unit polled for attention flag
        FIP                 4            FIFO insertion pointer
        FRP                 4            FIFO removal pointer
        FCNT                5            FIFO counter
```

```
CTL                 1          interrupt enable
FLG                 1          ready flag
FBF                 1          ready flag buffer
SRQ                 1          DMA service request
BUSY                1          visible busy status
CMDF                1          command follows flag
CMDP                1          command pending flag
EOC                 1          end of cylinder flag
EOD                 1          end of data flag
DBUF[0:127]        16          sector buffer
DPTR                8          sector buffer pointer
CTIME              24          command response time
DTIME              24          data transfer response time
STIME              24          seek time (per cylinder)
RTIME              24          rotation time
TIMEOUT            31          controller timeout
```

Error handling is as follows:

```
error               processed as

not attached        disk not ready (heads unloaded)

end of file         assume rest of disk is zero

OS I/O error        report error and stop
```

2.7 Magnetic Tape

2.7.1 12559C Magnetic Tape Controller (MTC, MTD) with One 3030 Drive

The 12559C magnetic tape drive has two separate devices, a data channel (MTD) and a command channel (MTC). The data channel includes a maximum record sized buffer for reads and writes. The command channel includes the tape unit. Magnetic tape options include the ability to make the unit write enabled or write locked.

```
SET MTC LOCKED              set unit write locked
SET MTC WRITEENABLED        set unit write enabled
```

The BOOT command is not supported. The 12559C was HP's earliest tape drive and is not supported by most of its operating systems. It is disabled by default.

The data channel (MTD) implements these registers:

```
name                size       comments

FLG                 1          channel ready
SRQ                 1          channel DMA service request
DBUF[0:65535]       8          transfer buffer
BPTR               16          buffer pointer (reads and writes)
BMAX               16          buffer size (writes)
```

The command channel (MTC) implements these registers:

```
name                size       comments
```

```
FNC                8              current function
STA                9              tape status
BUF                8              buffer
CTL                1              interrupt enabled
FLG                1              controller ready
FBF                1              controller ready buffer
SRQ                1              controller DMA service request
DTF                1              data transfer flop
FSVC               1              first service flop
POS                32             magtape position
CTIME              24             command delay time
XTIME              24             interword transfer delay time
STOP_IOE           1              stop on I/O error
```

Error handling is as follows:

```
error              processed as

not attached       tape not ready; if STOP_IOE, stop

end of file        parity error

OS I/O error       parity error; if STOP_IOE, stop
```

2.7.2 13181A Magnetic Tape Controller (MSC, MSD) with Four 7970B Drives, 13183A Magnetic Tape Controller (MSC, MSD) with Four 7970E Drives

The 13181A/13183A magnetic tape drive has two separate devices, a data channel (MTD) and a command channel (MTC). The data channel includes a maximum record sized buffer for reads and writes. The command channel includes the tape units. Magnetic tape options include the ability to select the 13181A (800 bpi) controller or the 13183A (1600 bpi) controller, and the ability to set a drive offline and online, write enabled or write locked.

```
SET MSC 13181A               set controller to 13181A
SET MSC 13183A               set controller to 13183A
SET MSCn OFFLINE             set unit n offline
SET MSCn ONLINE              set unit n online
SET MSCn LOCKED              set unit n write locked
SET MSCn WRITEENABLED        set unit n write enabled
SET MSC REALTIME             set controller to actual timing
SET MSC FASTTIME             set controller to optimized timing (default)
SET MSCn REEL=length         set unit tape reel size
                             0 = unlimited (default)
                             600 = 600 feet
                             1200 = 1200 feet
                             2400 = 2400 feet
SET MSCn CAPAC=m             set unit n capacity to m MB (0 = unlimited)
```

Setting the controller to optimized timing with SET MSC FASTTIME also enables two other optimizations: the initial gap normally written after BOT is omitted, and the Gap and File Mark (GFM) command is executed as a Write File Mark (WFM) command instead. Note that this does not affect the Write Gap (GAP) command.

MSC may be configured to send debugging information to the previously enabled debug output device using these commands:

```
SET MSC DEBUG                       provide debug printouts
SET MSC NODEBUG                     inhibit debug printouts
```

Three debug flags that control the reporting level are supported:

```
CMDS            Report command initiations and completions
CPU             Report words received from and sent to the CPU
RWS             Report tape library reads, writes, and status returns
```

The 13181A/13183A supports the BOOT command. BOOT MSC loads the IBL for 7970B/E magnetic tape drives into memory and starts it running. BOOT –S MSC causes the loader to position to the file number specified in the A register before starting to load data. The switch register (S) is set automatically to the value expected by the IBL loader:

```
<15:12>     =       1000
<11:6>      =       data channel device code
<5:3>       =       unchanged
<2:0>       =       00
<0>         =       1 if position tape before loading
```

The data channel (MSD) implements these registers:

```
name                size            comments

BUF                 16              data buffer
CTL                 1               interrupt enabled
FLG                 1               channel ready
FBF                 1               channel ready buffer
SRQ                 1               channel DMA service request
DBUF[0:65535]       8               transfer buffer
BPTR                17              buffer pointer (reads and writes)
BMAX                17              buffer size (writes)
```

The command channel (MSC) implements these registers:

```
name                size            comments

STA                 12              tape status
BUF                 16              buffer
USEL                2               currently selected unit
FSVC                1               first service flop
CTL                 1               interrupt enabled
FLG                 1               controller ready
FBF                 1               controller ready buffer
SRQ                 1               controller DMA service request
POS[0:3]            32              magtape position
BTIME               24              BOT start delay time
CTIME               24              command delay time
GTIME               24              gap traversal time
ITIME               24              IRG traversal time
RTIME               24              rewind initiation time
XTIME               24              interword transfer delay time
STOP_IOE            1               stop on I/O error
```

Error handling is as follows:

```
error              processed as

not attached       tape not ready; if STOP_IOE, stop

end of file        parity error

OS I/O error       parity error; if STOP_IOE, stop
```

3 Symbolic Display and Input

The HP2100 simulator implements symbolic display and input. Display is controlled by command line switches:

```
-a                 display as ASCII character
-c                 display as two packed ASCII characters
-m                 display instruction mnemonics
```

Input parsing is controlled by the first character typed in or by command line switches:

```
' or -a            ASCII character
" or -c            two packed ASCII characters
alphabetic         instruction mnemonic
numeric            octal number
```

Instruction input uses standard HP2100 assembler syntax. There are seven instruction classes: memory reference, I/O, shift, alter skip, extended shift, extended memory reference, extended two address reference.

Memory reference instructions have the format

```
memref {C/Z} address{,I}
```

where I signifies indirect, C a current page reference, and Z a zero page reference. The address is an octal number in the range 0 - 077777; if C or Z is specified, the address is a page offset in the range 0 - 01777. Normally, C is not needed; the simulator figures out from the address what mode to use. However, when referencing memory outside the CPU (e.g., disks), there is no valid PC, and C must be used to specify current page addressing.

IOG instructions have the format

```
io device{,C}
```

where C signifies that the device flag is to be cleared. The device is an octal number in the range 0 - 77.

Shift and alter/skip instructions have the format

```
sub-op sub-op sub-op...
```

The simulator checks that the combination of sub-opcodes is legal.

Extended shift instructions have the format

```
        extshift count
```

where count is an octal number in the range 1 - 020.

Extended memory reference instructions have the format

```
        extmemref address{,I}
```

where I signifies indirect addressing. The address is an octal number in the range 0 - 077777.

Extended two address instructions have the format

```
        ext2addr addr1{,I},addr2{,I}
```

where I signifies indirect addressing. Both address 1 and address 2 are octal numbers in the range 0 - 077777.